

What Is Claimed Is:

- 1 1. A method for latching and amplifying a capacitively coupled inter-
2 chip communication signal, comprising:
3 receiving an input signal on a capacitive receiver pad from a capacitive
4 transmitter pad;
5 feeding the input signal through an inverter to produce an output signal;
6 feeding the output signal through a weakened inverter to produce a
7 feedback signal; and
8 feeding the feedback signal back into an input of the inverter so as to form
9 a latch for the input signal between the inverter and the weakened inverter;
10 wherein the weakened inverter is biased to produce the feedback signal
11 that swings between a high bias voltage, V_H , and a low bias voltage, V_L ;
12 wherein V_H is slightly higher than a switching threshold of the inverter, and
13 V_L is slightly lower than the switching threshold of the inverter, whereby the
14 feedback signal causes the input signal to reside within a narrow voltage range
15 near the switching threshold of the inverter, thereby making the inverter sensitive
16 to small transitions in the input signal received on the capacitive receiver pad.
- 1 2. The method of claim 1, further comprising amplifying an output of
2 the inverter through an amplification stage to produce an amplified output signal.
- 1 3. The method of claim 2, further comprising establishing the high
2 bias voltage, V_H , with a high bias voltage generator and establishing the low bias
3 voltage, V_L , with a low bias voltage generator.
- 1 4. The method of claim 3,

2 wherein the high bias voltage generator includes a mechanism for
3 adjusting the high bias voltage, V_H ; and
4 wherein the low bias voltage generator includes a mechanism for adjusting
5 the low bias voltage, V_L .

1 5. The method of claim 4, further comprising adjusting the high bias
2 voltage generator and the low bias voltage generator to provide a specified
3 sensitivity to transitions of the input signal.

1 6. The method of claim 4, further comprising adjusting the high bias
2 voltage generator and the low bias voltage generator to provide a specified noise
3 immunity to noise associated with the input signal.

1 7. The method of claim 1, further comprising adjusting an RC time
2 constant for the feedback signal so that the time constant for the feedback signal is
3 significantly larger than the time constant for the transmitted signal from the
4 capacitive transmitter pad, thereby ensuring that the feedback signal does not
5 mask transitions of the transmitted signal.

1 8. An apparatus for latching and amplifying a capacitively coupled
2 inter-chip communication signal, comprising:
3 a receiving mechanism configured to receive an input signal on a
4 capacitive receiver pad from a capacitive transmitter pad; and
5 a latching mechanism configured to feed the input signal through an
6 inverter to produce an output signal;
7 wherein the latching mechanism is further configured to feed the output
8 signal through a weakened inverter to produce a feedback signal; and

9 wherein the latching mechanism is further configured to feed the feedback
10 signal back into an input of the inverter so as to form a latch for the input signal
11 between the inverter and the weakened inverter;
12 wherein the weakened inverter is biased to produce the feedback signal
13 that swings between a high bias voltage, V_H , and a low bias voltage, V_L ;
14 wherein V_H is slightly higher than a switching threshold of the inverter, and
15 V_L is slightly lower than the switching threshold of the inverter, whereby the
16 feedback signal causes the input signal to reside within a narrow voltage range
17 near the switching threshold of the inverter, thereby making the inverter sensitive
18 to small transitions in the input signal received on the capacitive receiver pad.

1 9. The apparatus of claim 8, further comprising an amplifying
2 mechanism configured to amplify an output of the inverter through an
3 amplification stage to produce an amplified output signal.

1 10. The apparatus of claim 9, further comprising a biasing mechanism
2 configured to establishing the high bias voltage, V_H , with a high bias voltage
3 generator and establishing the low bias voltage, V_L , with a low bias voltage
4 generator.

1 11. The apparatus of claim 10,
2 wherein the high bias voltage generator includes a mechanism for
3 adjusting the high bias voltage, V_H , and
4 wherein the low bias voltage generator includes a mechanism for the low
5 bias voltage, V_L .

1 12. The apparatus of claim 11, further comprising an adjusting
2 mechanism configured to adjust the high bias voltage generator and the low bias
3 voltage generator to provide a specified sensitivity to transitions of the input
4 signal.

1 13. The apparatus of claim 11, further comprising an adjusting
2 mechanism configured to adjust the high bias voltage generator and the low bias
3 voltage generator to provide a specified noise immunity to noise associated with
4 the input signal.

1 14. The apparatus of claim 8, further comprising an adjusting
2 mechanism configured to adjust an *RC* time constant for the feedback signal so
3 that the time constant for the feedback signal is significantly larger than the time
4 constant for the transmitted signal from the capacitive transmitter pad, thereby
5 ensuring that the feedback signal does not mask transitions of the transmitted
6 signal.

1 15. A means for latching and amplifying a capacitively coupled inter-
2 chip communication signal, comprising:
3 a receiving means for receiving an input signal on a capacitive receiver
4 pad from a capacitive transmitter pad; and
5 a latching means configured to feed the input signal through an inverter to
6 produce an output signal;
7 wherein the latching means is further configured to feed the output signal
8 through a weakened inverter to produce a feedback signal; and

9 wherein the latching means is further configured to feed the feedback
10 signal back into an input of the inverter so as to form a latch for the input signal
11 between the inverter and the weakened inverter;
12 wherein the weakened inverter is biased to produce the feedback signal
13 that swings between a high bias voltage, V_H , and a low bias voltage, V_L ;
14 wherein V_H is slightly higher than a switching threshold of the inverter, and
15 V_L is slightly lower than the switching threshold of the inverter, whereby the
16 feedback signal causes the input signal to reside within a narrow voltage range
17 near the switching threshold of the inverter, thereby making the inverter sensitive
18 to small transitions in the input signal received on the capacitive receiver pad.

1 16. The means of claim 15, further comprising an amplifying means
2 for amplifying an output of the inverter through an amplification stage to produce
3 an amplified output signal.

1 17. The means of claim 16, further comprising a biasing means for
2 establishing the high bias voltage, V_H , with a high bias voltage generator and for
3 establishing the low bias voltage, V_L , with a low bias voltage generator.

1 18. The means of claim 17,
2 wherein the high bias voltage generator includes a mechanism for
3 adjusting the high bias voltage, V_H ; and
4 wherein the low bias voltage generator includes a mechanism for the low
5 bias voltage, V_L .

1 19. The means of claim 18, further comprising an adjusting means for
2 adjusting the high bias voltage generator and the low bias voltage generator to
3 provide a specified sensitivity to transitions of the input signal.

1 20. The means of claim 18, further comprising an adjusting means for
2 adjusting the high bias voltage generator and the low bias voltage generator to
3 provide a specified noise immunity to noise associated with the input signal.

1 21. The means of claim 15, further comprising an adjusting means for
2 adjusting an *RC* time constant for the feedback signal so that the time constant for
3 the feedback signal is significantly larger than the time constant for the
4 transmitted signal from the capacitive transmitter pad, thereby ensuring that the
5 feedback signal does not mask transitions of the transmitted signal.